**# Title:**

Add MADT GIC Flags for non-coherent components.

**# Status:**

Draft

**# Document:**

ACPI 6.5 specification

**# License:**

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**# Submitters:**

* Arm Limited
* TianoCore Community (<https://www.tianocore.org>)

**# Summary of the change**

The GICv3+ architecture specifications provide a means for the system programmer to set the shareability and cacheability attributes that the GIC components (Redistributors and ITSes) use to drive memory transactions. However, it is possible for the GIC Redistributors and ITSes to be wired up, or connected to non-coherent interconnects, such that the affected GIC components become non-coherent. OSPM needs to detect this scenario, and use appropriate the Cache Maintenance Operations (CMOs) on the GIC Memory tables.

To enable non-coherent GIC designs, introduce a new GIC CPU i/f, GICR and GIC ITS flag to allow the firmware to describe Redistributors and ITSes as non-coherent observers, and use this property to force the shareability attributes to be programmed by OSPM into the Redistributor and ITS registers as non-shareable.

**Note**: We are not allowing different redistributors to have different coherency attributes, since we do not think that is a sensible configuration. However, there is no similar restriction on ITSs.

**# Benefits of the change**

Adds support for systems which have non-coherent GICR and GIC-ITS.

**# Impact of the change**

* There is no impact to existing systems, or systems where the GIC components are coherent.
* Systems where GICR or GIC ITS is non-coherent will need to upgrade to this version 7 of MADT for OSPM to work correctly.

**# Detailed description of the change [normative updates]**

* Insertions in green
* Removals in ~~red~~
* Cross-reference highlighted

Table 5-19 Multiple APIC Description Table (MADT) Format

|  |  |  |  |
| --- | --- | --- | --- |
| Field | Byte Length | Byte Offset | Description |
| Header |  |  |  |
| **…** | **…** | **…** | **…** |
| Revision | 1 | 8 | ~~6~~ 7 |
| **…** | **…** | **...** | **…** |

Table 5.37: GICC CPU Interface Flags

|  |  |  |  |
| --- | --- | --- | --- |
| GIC Flags | Bit Length | Bit Offset | Description |
| Enabled | 1 | 0 | … |
| … | … | … | … |
| Online Capable | 1 | 3 | … |
| GICR Non-coherent | 1 | 4 | ﻿On systems supporting GICv3 and above, this field specifies if the GIC Redistributor described in the associated GICC structure is cache coherent with the CPU. The values for this flag are:  0x0: This Redistributor is fully coherent. OSPM does not need to perform any Cache Maintenance on the associated tables in memory if the appropriate cacheability and shareability attributes have been configured in the Redistributor.  0x1: This Redistributor is not coherent. OSPM needs to perform cache maintenance on the associated tables in memory.  If all the GIC Redistributors are in the always-on power domain, then the GICR structure is used to describe this Redistributor and this field must be ignored by OSPM.  Note: All GIC CPU Interface structures in the system must have the same value for this flag. |
| Reserved | ~~28~~ 27 | ~~4~~ 5 | Must be zero. |

Table 5.41: GICR Structure

|  |  |  |  |
| --- | --- | --- | --- |
| Field | Byte Length | Byte Offset | Description |
| Type | 1 | 0 | 0xE GICR Structure |
| Length | 1 | 1 | 16 |
| Flags | 1 | 2 | See GICR Flags |
| Reserved | ~~2~~ 1 | ~~2~~ 3 | Reserved – Must be Zero |
| Discovery Range Base Address | 8 | 4 | … |
| … | … | … | … |

Table 5.xx: GICR Flags

|  |  |  |  |
| --- | --- | --- | --- |
| GICR Flags | Bit Length | Bit Offset | Description |
| GICR Non-coherent | 1 | 0 | ﻿This field specifies if the associated GIC Redistributors are cache coherent with the CPU. The values for this flag are:  0x0: The Redistributors are fully coherent. OSPM does not need to perform any Cache Maintenance on the associated tables in memory if the appropriate cacheability and shareability attributes have been configured in the Redistributors.  0x1: The Redistributors are not coherent. OSPM needs to perform cache maintenance on the associated tables in memory.  Note: If there are multiple GICR structures present in MADT, then all the GICR structures must have the same value for this flag. |
| Reserved | 7 | 1 | Must be zero. |

Table 5.42: GIC ITS Structure

|  |  |  |  |
| --- | --- | --- | --- |
| Field | Byte Length | Byte Offset | Description |
| Type | 1 | 0 | 0xF GIC ITS Structure |
| Length | 1 | 1 | 20 |
| Flags | 1 | 2 | See GIC ITS Flags |
| Reserved | ~~2~~ 1 | ~~2~~ 3 | Reserved – Must be Zero |
| GIC ITS ID | 4 | 4 | … |
| … | … | … | … |

Table 5.xx: GIC ITS Flags

|  |  |  |  |
| --- | --- | --- | --- |
| GIC ITS Flags | Bit Length | Bit Offset | Description |
| GIC ITS Non-coherent | 1 | 0 | ﻿This field specifies if the associated GIC ITS is cache coherent with the CPU. The values for this flag are:  0x0: This ITS is fully coherent. OSPM does not need to perform any Cache Maintenance on the associated tables in memory if the appropriate cacheability and shareability attributes have been configured in the ITS.  0x1: This ITS is not coherent. OSPM needs to perform cache maintenance on the associated tables in memory. |
| Reserved | 7 | 1 | Must be zero. |